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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/464,322	12/15/1999	HEUNG-KYU KWON	AB-881US	7367
30593 7590 05/02/2007 HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910			EXAMINER	
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RESTON, VA 20195			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
· .	09/464,322	KWON ET AL.				
Office Action Summary	Examiner	Art Unit				
-	Chris C. Chu	2815				
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet v	vith the correspondence address				
	DIVIQUET TO EVOIDE 2 M	AONTH(S) OF THIRTY (20) DAVS				
A SHORTENED STATUTORY PERIOD FOR REF WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the main earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUN 1.136(a). In no event, however, may a od will apply and will expire SIX (6) MO ute, cause the application to become A	ICATION. reply be timely filed NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on <u>07</u>	February 2007.					
3) Since this application is in condition for allow	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice unde	r <i>Ex par</i> te Quayle, 1935 C.	D. 11, 453 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>2 - 15 and 17 - 20</u> is/are pending in	the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>2 - 15 and 17 - 20</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and	I/or election requirement.					
Application Papers	•					
9) The specification is objected to by the Exami	ner.					
10)⊠ The drawing(s) filed on <u>28 June 2001</u> is/are: a) accepted or b)⊠ objected to by the Examiner.						
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the corre						
11)☐ The oath or declaration is objected to by the	Examiner. Note the attache	ed Office Action or form PTO-152.				
Priority under 35 U.S.C. § 119		,				
12) Acknowledgment is made of a claim for forei	gn priority under 35 U.S.C.	§ 119(a)-(d) or (f).				
a)⊠ All b)□ Some * c)□ None of:						
 Certified copies of the priority docume 	1. Certified copies of the priority documents have been received.					
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the pr	· ·	n received in this National Stage				
application from the International Bure	, , , , , , , , , , , , , , , , , , , ,					
* See the attached detailed Office action for a li	ist of the certified copies no	ot received.				
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 		Summary (PTO-413) o(s)/Mail Date				
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date		Informal Patent Application				

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on February 7, 2007 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitation in claim 8 "the heat slug comprises a solder bonding layer formed on a surface of the heat slug that contacts the solder film" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

On page 7, applicant argues "the drawings do <u>not</u> require any changes as Fig. 1 discloses the features recited in claim 8. Namely, reference character "42" is an 'adhesion layer' that may be formed on one side 41 of the heat slug 40." This argument is not persuasive because the claim

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8 specifically discloses "a solder bonding layer formed on a surface of the heat slug that contacts the solder film." However, the reference character "42" in Fig. 1 is an "adhesion layer", not a "solder bonding layer". Thus, the Fig. 1 of instant invention does not show the following limitation in claim 8 "the heat slug comprises a solder bonding layer formed on a surface of the heat slug that contacts the solder film". Thus, the objection of the drawing is maintained.

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Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 3, 5, 6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (U. S. Pat. No. 5,592,735) in view of Akasaki et al. (U. S. Pat. No. 5,217,922).

Regarding claim 3, Ozawa et al. discloses in Fig. 14 a semiconductor chip package comprising:

- a substrate (41) having a plurality of bonding pads;
- a semiconductor chip (32-2) having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;
- a heat slug (36) bonded to a backside of the semiconductor chip; and
- a solder film (144) directly attached to the heat slug (36) thereby bonding the heat slug to the backside of the semiconductor chip,

- wherein the backside of the semiconductor chip includes a solder bonding metal layer (33-2) "in contact with" and between the semiconductor chip and the solder film.

Further, the recitation "a plurality of bonding pads" is structurally inherent in Ozawa et al.

However, Ozawa et al. does not disclose a multi-metal layer film in contact with and between the semiconductor chip and the solder film. Akasaki et al. teaches in e.g., Fig. 2(F) a multi-metal layer film (15-17 or 9A; column 5, lines 49-62 and see e.g., Fig. 2(F)) in contact with and between a semiconductor chip (1; column 5, line 3) and a solder film (8; column 7, lines 20 and 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ozawa et al. by using the multi-metal layer film as taught by Akasaki et al. The ordinary artisan would have been motivated to modify Ozawa et al. in the manner described above for at least the purpose of increasing adhesion to the back of a silicone substrate without thermal damage to a BLM layer or a semiconductor element (column 2, lines 23-27).

Regarding claim 5, Ozawa et al. discloses in Fig. 14 a space between the semiconductor chip and the substrate being filled with an underfilling material (141).

Regarding claim 6, Ozawa et al. discloses in Fig. 14 the solder film (144) having a size equal to or larger than a size of the semiconductor chip (32-2).

Regarding claim 14, the method steps are disclosed by Ozawa et al. for the same reasons provided above with regarding claim 3.

Regarding claim 15, Ozawa et al. discloses in Fig. 14 filling a resin (141) into a space between the semiconductor chip and the substrate.

5. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Haley.

Regarding claim 2, Ozawa et al. and Akasaki et al. disclose the claimed invention except for the material of the solder film, which includes one selected from "a group consisting of Pb, Sn, Ag, In, and Bi." However, Haley discloses in column 3, lines 66 –67 the material of a solder film. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by selecting from a group consisting of Pb, Sn, Ag, In, and Bi for the material of the solder film as taught by Haley. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of increasing the bond strength between the semiconductor chip and the heat slug.

Regarding claim 13, Ozawa et al. and Akasaki et al. disclose the claimed invention except for a plurality of "throughholes" on the heat slugs. However, Haley discloses the plurality of "throughholes" on the heat slugs (108 and 109 in Fig. 1). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by adding the plurality of "throughholes" on the heat slugs as taught by Haley. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of decreasing moisture inside of the package.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Furukawa et al.

Ozawa et al. and Akasaki et al. disclose the claimed invention except for the material of the metal layer, which includes one selected from "a group consisting of VNi/Au, Ti/VNi/Au, Cr/Vni/Au, Ti/Pt/Au, and etc." However, Furukawa et al. discloses the material of the metal layer (column 9, lines 63 –64). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further rmodify Ozawa et al. and Akasaki et al. by selecting from a group consisting of VNi/Au, Ti/VNi/Au, Cr/Vni/Au, Ti/Pt/Au, and etc for the material of the metal layer as taught by Furukawa et al. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of increasing the bond strength between the semiconductor chip and the solder film.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Takahama et al.

Ozawa et al. and Akasaki et al. disclose the claimed invention except that the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW. However, Takahama et al. discloses that the material of the heat slug (column 6, lines 38 – 39). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by selecting from a group consisting as of Cu, Al, and CuW as taught by Takahama et al. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of improving heat dissipation.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Myers et al.

Regarding claim 8, Ozawa et al. and Akasaki et al. disclose the claimed invention except for the heat slug comprises a solder bonding layer formed on a surface of the heat slug that contacts the solder film. However, Myers et al. discloses in Fig. 2 a heat slug (32) comprising a solder bonding layer (30) formed on a surface of the heat slug (32) that contacts a solder film (28). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by using the solder bonding layer as taught by Myers et al. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of spreading heat laterally (column 1, lines 64 ~ 66).

Regarding claim 9, Myers et al. discloses in column 1, lines 64 and 65 the solder bonding layer being a Ag layer.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Jeong et al.

Ozawa et al. and Akasaki et al. disclose the claimed invention except for the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded. However, Jeong et al. discloses that an anodizing layer (73b in Fig. 6 and column 8, lines 2-5 and read column 7, lines $65 \sim 67$) on a surface of a heat slug (73) that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded (see Fig. 6). Thus, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by using the anodizing layer as taught by Jeong et al. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of increasing the corrosion resistant and electrical insulation.

10. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. and Akasaki et al. as applied to claim 3 above, and further in view of Hawthorne et al.

Regarding claim 11, Ozawa et al. and Akasaki et al. disclose the claimed invention except for the heat slug being shaped such that a portion of the heat slug is attached to the substrate by an adhesive. However, Hawthorne et al. discloses in Fig. 3 the heat slug being shaped such that a portion of the heat slug (66) is attached to the substrate (40, 50a and 50b) by an adhesive (62). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Ozawa et al. and Akasaki et al. by using the shape of the heat slug as taught by Hawthorne et al. The ordinary artisan would have been motivated to further modify Ozawa et al. and Akasaki et al. in the manner described above for at least the purpose of increasing reliability of package.

Regarding claim 12, Ozawa et al., Akasaki et al. and Hawthorne et al. discloses the claimed invention except for the adhesive includes silicon rubber or elastomer. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to using silicon rubber or elastomer material for the adhesive, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. The ordinary artisan would

have been motivated to further modify Ozawa et al. in the manner described above for at least the purpose of increasing the bond strength between the heat slug and the substrate. In re Leshin, 125 USPQ 416.

11. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hawthorne et al. in view of Ozawa et al., and further in view of Akasaki et al.

Regarding claim 17, Hawthorne et al. discloses in Fig. 3 the solder film (71) has a size equal to or larger than a size of the semiconductor chip (44).

Regarding claim 19, Hawthorne et al. discloses in Fig. 3 a semiconductor chip package comprising:

- a substrate (40, 50a and 50b) having a plurality of bonding pads (see Fig. 3);
- a semiconductor chip (44) having a plurality of conductive bumps (54) on a front side thereof, the conductive bumps (54) contacting the bonding pads (see Fig. 3);
- a heat slug (66) bonded to the semiconductor chip (see Fig. 3), the heat slug (66) comprising a top portion, side standing portions bent from the top portion, and side end portions bent again from the side standing portions (see Fig. 3); and
- a conductive solder film (71) that bonds the heat slug (66) to the backside of the semiconductor chip (see Fig. 3), wherein the heat slug (66) contacts the solder film (71) and the side end portions (70) of the heat slug (66) are attached to the substrate (40, 50a and 50b) by an adhesive (62 and see Fig. 3).

Hawthorne et al. does not disclose a solder bonding layer formed on a surface of the heat slug that contacts the solder film and the backside of the semiconductor chip includes a solder

bonding metal layer in contact with and between the semiconductor chip and the solder film. However, Ozawa et al. discloses in Fig. 14 a heat slug (47) comprising a solder bonding layer (42) formed on a surface of a heat slug (47) that contacts (thermal contact) a solder film (144) and backside of a semiconductor chip (32-2) including a solder bonding metal layer (33-2) in contact with and between the semiconductor chip and the solder film. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hawthorne et al. by using the solder bonding layer and the solder bonding metal layer as taught by Ozawa et al. The ordinary artisan would have been motivated to modify Hawthorne et al. in the manner described above for at least the purpose of reducing thermal resistance and improving heat radiation (column 2, lines 19 ~ 22). Further, the recitation "a plurality of bonding pads" is structurally inherent in Hawthorne et al.

However, Hawthorne et al. and Ozawa et al. do not disclose a multi-metal layer film in contact with and between the semiconductor chip and the solder film. Akasaki et al. teaches in e.g., Fig. 2(F) a multi-metal layer film (15 – 17 or 9A; column 5, lines 49 – 62 and see e.g., Fig. 2(F)) in contact with and between a semiconductor chip (1; column 5, line 3) and a solder film (8; column 7, lines 20 and 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hawthorne et al. and Ozawa et al. by using the multi-metal layer film as taught by Akasaki et al. The ordinary artisan would have been motivated to further modify Hawthorne et al. and Ozawa et al. in the manner described above for at least the purpose of increasing adhesion to the back of a silicone substrate without thermal damage to a BLM layer or a semiconductor element (column 2, lines 23 – 27).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawthorne et al., Ozawa et al. and Akasaki et al. as applied to claim 19 above, and further in view of Takahama et al.

Hawthorne et al., as modified, discloses the claimed invention except that the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW. However, Takahama et al. discloses in column 6, lines 38 – 39 the material of the heat slug. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hawthorne et al. by selecting from a group consisting as of Cu, Al, and CuW as taught by Takahama et al. The ordinary artisan would have been motivated to further modify Hawthorne et al. in the manner described above for at least the purpose of improving heat dissipation.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawthorne et al., Ozawa et al. and Akasaki et al. as applied to claim 19 above, and further in view of Jeong et al.

Hawthorne et al., as modified, discloses the claimed invention except for the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded. However, Jeong et al. discloses that an anodizing layer (73b in Fig. 6 and column 8, lines 2-5 and read column 7, lines $65 \sim 67$) on a surface of a heat slug (73) that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded (see Fig. 6). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hawthorne et al. by using the anodizing layer as taught by Jeong et al. The ordinary artisan would have been motivated to

further modify Hawthorne et al. in the manner described above for at least the purpose of increasing the corrosion resistant and electrical insulation.

Response to Arguments

14. Applicant's arguments filed on February 7, 2007 have been fully considered but they are not persuasive.

On page 5, applicant argues "Ozawa an Akasaki are <u>not</u> combinable, and the Examiner has failed to provide a proper evidence of a suggestion or motivation for the combination." This argument is not persuasive. First, Ozawa' objection is reducing thermal resistance and a substantially improved heat radiation. The multi-metal layer film (15 – 17) of Akasaki et al. provides better attachment between the semiconductor chip and the solder film without thermal damage to the semiconductor element. In other words, the multi-metal layer film (15 – 17) of Akasaki et al. reduces thermal resistance and provides a heat radiation between the heat sink and the semiconductor element without thermal damage to the semiconductor element. Thus, by adding the multi-metal layer film (15 – 17 of Akasaki et al.) between the semiconductor chip (32-2) and the solder film (144) of Ozawa reduces a thermal resistance and a substantially improved heat radiation without thermal damage to the semiconductor element. Thus, Ozawa an Akasaki are combinable.

Furthermore, applicant shoud note that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071,

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5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Contrary to applicant's assertion and as stated in the rejection, motivation was established by Akasaki et al., specifically in column 2, lines 23 – 27 (increasing adhesion to the back of a silicone substrate without thermal damage to a BLM layer or a semiconductor element).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, Akasaki et al. reference clearly teaches with specific reasons why the multi-metal layer film (15 – 17 of Akasaki et al.) is needed between the semiconductor chip and the solder film as well as additional benefits afforded by that invention. Thus, the motivation is proper to use in a combination of the multi-metal layer film of Akasaki et al. between the semiconductor chip and the solder film of Ozawa.

For the above reasons, the rejection is maintained.

Conclusion

15. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu Examiner Art Unit 2815

c.c. Thursday, April 26, 2007

KENNETH PARKER
SUPERVISORY PATENT EXAMINA